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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,318	12/30/2003	Jae-Geun Oh	00939H-087500US	1692

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EXAMINER	
SMITH, BRADLEY	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,318	OH ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Official Notice

1. Official notice is taken that the gradient of a scalar function is mathematically equivalent to the slope of the function. This statement is supported by the reference, *CRC Standard Mathematical Tables and Formulae*.

Official notice is taken that higher energy ions are necessary to penetrate an overlying screening layer since the ions loose energy within the layer. This statement is supported by the references *Silicon Processing for the VLSI Era* and *Electronic Materials Science*.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

JKS 12/7/06

3. Claims ~~1—21~~ 1-9 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran *et al.* in view of Fischer *et al.*

Regarding claims 1, 2, and 6, Tran *et al.* (US 6,759,288) teaches a method for forming plugs on active regions of a semiconductor device comprising the steps of forming a plurality of gate lines **16** on a substrate **12**, implanting a first dopant **25** using the gate lines as a mask [column 11, line 10] to form a plurality of cell junctions **202** with gate lines formed between the cell junctions, forming a buffer layer **72** over the cell junctions, implanting a second dopant **26** under the buffer layer, forming contact plugs 82, where the concentration profile has a reduced

slope which suppresses the width of the depletion layer [column 12, lines 10-15; column 10, lines 30-40] and the buffer (screening) layer intrinsically enables a higher implantation energy, as described by Wolf (*Silicon Processing for the VLSI Era*). Tran *et al.* teaches implanting a second dopant with the same conductivity type but not necessarily of a different energy or forming a well implantation. Fischer *et al.* (US 6,693,014) teaches forming cell junctions with a second implantation that has a higher energy than the first implantation [Figure 6] and a well implantation formed before the cell and plug implantations [column 2, lines 1-10]. It would have been obvious to one of ordinary skill in the art to use the implantation energies and well implantation of Fischer *et al.* in the method of Tran *et al.* since the higher implant energy provides a device with improved static refresh performance and the well implantation is a standard MOSFET design for improving DRAM device performance.

Regarding claim 3, Tran *et al.* further teaches a phosphorus implantation with a dose range of 5×10^{11} to 5×10^{12} ions/cm^2 with an energy of 30 – 100 KeV [column 8, lines 1-5].

Regarding claim 4, Tran *et al.* further teaches an energy distribution applied in several sets [Figure 16].

Regarding claim 5, Tran *et al.* does not discuss several sets of increasing energy from a high level to a low level. Fischer *et al.* teaches an ion implantation method where several sets of dopants are implanted with increasing energy from a high level to a low level [Figure 6]. It would have been obvious to one of ordinary skill in the art to use the implantation method of Fischer *et al.* in the method of Tran *et al.* since this method improves the threshold voltage of the resulting device.

Regarding claim 7, Tran *et al.* further teaches a nitride layer with a thickness of 30 – 200 Å [column 11, lines 30-45].

Regarding claim 8, Tran *et al.* further teaches N type dopants [column 11, lines 25 and 55].

Regarding claim 9, Tran *et al.* further teaches forming a spacer by etching the buffer layer [Figure 23], forming an interlayer insulation layer **32, 34**, forming a plurality of contact holes [Figure 23], and forming a plurality of contact plugs **82**.

Regarding claim 21, Tran *et al.* teaches a method for forming plugs on active regions of a semiconductor device comprising the steps of forming a plurality of gate lines **16** on a substrate **12**, forming a plurality of cell junctions **202** by ion implanting a first dopant **25** using the gate lines as a mask [column 11, line 10], forming a buffer layer **72**, and forming a plurality of plug regions **212** by ion implanting a second dopant **26** under the buffer layer, where the concentration profile has a reduced slope [column 12, lines 10-15] and the buffer layer intrinsically enables a higher implantation energy, as described by Wolf (*Silicon Processing for the VLSI Era*). Tran *et al.* does not teach forming a well implantation. Fischer *et al.* teaches forming a well implantation formed before the cell and plug implantations [column 2, lines 1-10]. It would have been obvious to one of ordinary skill in the art to use the well implantation of Fischer *et al.* in the method of Tran *et al.* since the well implantation is a standard MOSFET design for improving DRAM device performance.

Regarding claims 19, and 20, Tran *et al.* teaches a method for forming plugs on active regions of a semiconductor device comprising the steps of forming a plurality of gate lines **16** on

a substrate **12**, implanting a first dopant **25** using the gate lines as a mask [column 11, line 10] to form a plurality of cell junctions **202** with gate lines formed between the cell junctions, forming a buffer layer **72** over the cell junctions, implanting a second dopant **26** under the buffer layer, where the concentration profile has a reduced slope which suppresses the width of the depletion layer [column 12, lines 10-15; column 10, lines 30-40] and the buffer layer intrinsically enables a higher implantation energy, as described by Wolf (*Silicon Processing for the VLSI Era*). Tran *et al.* teaches implanting a second dopant with the same conductivity type but not necessarily of a different energy or forming a well implantation. Fischer *et al.* teaches forming cell junctions with a second implantation that has a higher energy than the first implantation [Figure 6] and a well implantation formed before the cell and plug implantations of a second conductivity type [column 2, lines 1-10]. It would have been obvious to one of ordinary skill in the art to use the implantation energies and well implantation of Fischer *et al.* in the method of Tran *et al.* since the higher implant energy provides a device with improved static refresh performance and the well implantation is a standard MOSFET design for improving DRAM device performance.

Response to Arguments

Applicant's arguments filed 7/17/06 have been fully considered but they are not persuasive. The applicant remarks that Tran fails to use the buffer layer to increase the implantation energy. However the examiner has clearly pointed out that it is well known in the art that the buffer (screening) layer would increase the implantation energy. Furthermore, since the prior art has already disclosed the method and the device being formed, the mere recitation of the dopants having a more evenly distributed profile and would enable a higher implant energy is not found persuasive. Tran would inherently have formed the same structure. Thus the

claiming of a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable. In re Best, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bradley K Smith
Primary Examiner
Art Unit 2891